10/616,303

Exhibit A

US006725356B2

(12) **United States Patent**
Hansen et al.

(10) **Patent No.: US 6,725,356 B2**
(45) **Date of Patent: *Apr. 20, 2004**

(54) **SYSTEM WITH WIDE OPERAND ARCHITECTURE, AND METHOD**

(75) Inventors: **Craig Hansen**, Los Altos, CA (US); **John Moussouris**, Palo Alto, CA (US)

(73) Assignee: **MicroUnity Systems Engineering, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: 09/922,319

(22) Filed: Aug. 2, 2001

(65) **Prior Publication Data**

US 2002/0133682 A1 Sep. 19, 2002

Related U.S. Application Data

(60) Continuation of application No. 09/382,402, filed on Aug. 24, 1999, now Pat. No. 6,295,599, which is a continuation-in-part of application No. 09/169,963, filed on Oct. 13, 1998, now Pat. No. 6,006,318, which is a continuation of application No. 08/754,827, filed on Nov. 22, 1996, now Pat. No. 5,822,603, which is a division of application No. 08/516,036, filed on Aug. 16, 1995, now Pat. No. 5,742,840.

(60) Provisional application No. 60/097,635, filed on Aug. 24, 1998.

(51) **Int. Cl.**[7] **G06F 15/00**

(52) **U.S. Cl.** **712/210**; 712/28; 712/24; 712/32; 712/208

(58) **Field of Search** 712/32, 28, 34, 712/208, 210, 20, 24

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,025,772 A 5/1977 Constant
4,489,393 A 12/1984 Kawahara et al.
4,701,875 A 10/1987 Konishi et al.

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

DE 0 654 733 A1 5/1994
JP 0 474 246 A2 6/1991

OTHER PUBLICATIONS

Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987.
Organization of the Motorola 88110 Superscalar RISC Microprocessor, Keith Diefendorff and Michael Allen.
Microprocessor Report, vol. 7 No. 13, Oct. 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.

(List continued on next page.)

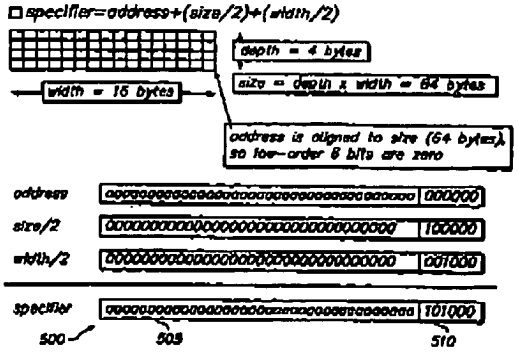
Primary Examiner—Matthew C. Bella
Assistant Examiner—Mackly Monestime
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

The present invention provides a system and method for improving the performance of general purpose processors by expanding at least one source operand to a width greater than the width of either the general purpose register or the data path width. In addition, the present invention provides several classes of instructions which cannot be performed efficiently if the operands are limited to the width and accessible number of general purpose registers. The present invention provides operands which are substantially larger than the data path width of the processor by using a general purpose register to specify a memory address from which at least more than one, but typically several data path widths of data can be read. The present invention also provides for the efficient usage of a multiplier array that is fully used for high precision arithmetic, but is only partly used for other, lower precision operations.

48 Claims, 148 Drawing Sheets

Microfiche Appendix Included
(5 Microfiche, 63 Pages)



U.S. PATENT DOCUMENTS

4,727,505	A		2/1988	Konishi et al.
4,876,660	A		10/1989	Owens et al.
4,893,267	A		1/1990	Alsup et al.
4,956,801	A		9/1990	Priem et al.
4,969,118	A		11/1990	Montoye et al.
4,975,868	A		12/1990	Fraerkson
5,032,865	A		7/1991	Schlunt
5,157,388	A		10/1992	Kohn
5,201,056	A		4/1993	Daniel et al.
5,268,855	A		12/1993	Mason et al.
5,268,995	A		12/1993	Diefendorff et al.
5,280,598	A	*	1/1994	Osaki et al. 710/127
5,408,581	A		4/1995	Suzuki et al.
5,423,051	A		6/1995	Fuller et al.
5,426,600	A		6/1995	Nakagawa et al.
5,487,024	A	*	1/1996	Girardeau, Jr. 708/606
5,500,811	A		3/1996	Corry
5,557,724	A		9/1996	Sampat et al.
5,588,152	A		12/1996	Dapp et al.
5,592,405	A		1/1997	Gove et al.
5,600,814	A	*	2/1997	Gahan et al. 711/100
5,640,543	A		6/1997	Farrell et al.
5,642,306	A		6/1997	Mennemeier et al.
5,666,298	A		9/1997	Peleg et al.
5,669,010	A		9/1997	Duluk, Jr.
5,673,407	A		9/1997	Poland et al.
5,675,526	A		10/1997	Peleg et al.
5,680,338	A		10/1997	Agarwal et al.
5,721,892	A		2/1998	Peleg et al.
5,734,874	A		3/1998	Van Hook et al.
5,757,432	A		5/1998	Dulong et al.
5,758,176	A		5/1998	Agarwal et al.
5,768,546	A	*	6/1998	Kwon 710/127
5,802,336	A		9/1998	Peleg et al.
5,809,292	A		9/1998	Wilkinson et al.
5,818,739	A		10/1998	Peleg et al.
5,825,677	A		10/1998	Agarwal et al.
5,835,782	A		11/1998	Lin et al.
5,886,732	A		3/1999	Humpleman
5,922,066	A		7/1999	Cho et al.
5,983,257	A		11/1999	Dulong et al.
6,016,538	A		1/2000	Gulag et al.
6,092,094	A		7/2000	Ireton
6,295,599	B1	*	9/2001	Hansen et al. 712/32
6,401,194	B1		6/2002	Nguyen et al.

OTHER PUBLICATIONS

IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, Jul. 31, 1995.

The Visual Instruction Set (VSI) in UltraSPAR™, L. Kohn, G. Maturana, M. Tremblay, A. Prabhu, G. Zyner, May 3, 1995.

Osborne McGraw-Hill, i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn.

A General-Purpose Array Processor for Seismic Processing, Nov.-Dec., 1984, vol. 1, No. 3) Revisiting past digital signal processor technology, Don Shaver- Jan.-Mar. 1998.

Accelerating Multimedia with Enhanced Microprocessors, Ruby B. Lee, 1995.

* cited by examiner

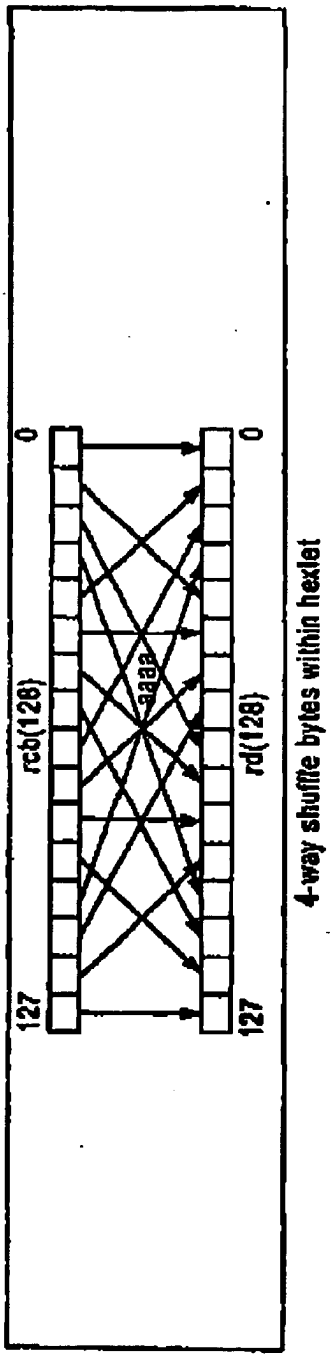


FIG. 34D

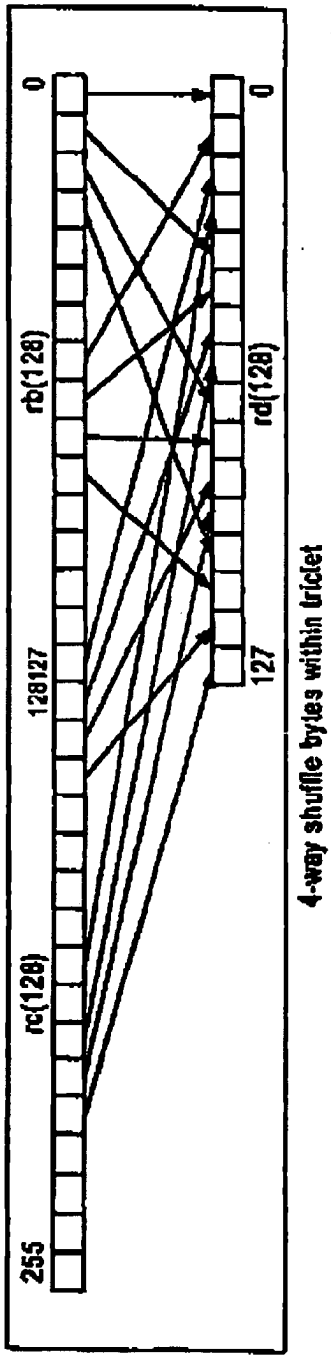


FIG. 34E